Page 2, paragraph beginning at line 6, has been r writt n as indicated below:

As a method of overcoming these disadvantages, for example, reference may be made to the technique disclosed in 2000 International Solid-State Circuits Conference Digest of Technical Papers, pp.294-295 (February, 2000). This technique is arranged so that a processor that is operated at high speed and low electric power may be realized by controlling the operating clock frequency and the supply voltage of a microprocessor composed of a CMOS circuit. If fast operation is required, by enhancing the clock frequency and the supply voltage, the operating speed may be improved while making the power consumption larger. On the other hand, if slow operation is allowed, by lowering the clock frequency and the supply voltage, the power consumption may be reduced. The combinational adjustment of these controls through the operating system realizes the fast operation and the low power consumption of the microprocessor.

A3

In the Claims:

Please cancel claims 1-16 without prejudice.

Please add new claims 17-35 as follows:

Sub B1 A4

– 17. A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit; and

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed,

wherein the frequency of the clock signal, the supply voltage and the

substrate bias voltage are adjusted according to an operating performance of the first circuit, and

wherein initial values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are decided based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage.

18. The semiconductor integrated circuit device according to claim 17, further comprising:

a command generating circuit to control the second circuit, the third circuit and the fourth circuit; and

A4 cont.

wherein the command generating circuit generates first, second and third command signals according to the operating performance of the first circuit,

the second circuit sets a frequency of the clock signal in response to the first command signal,

the third circuit sets a value of the supply voltage in response to the second command signal, and

the fourth circuit sets a value of the substrate bias voltage in response to the third command signal.

19. A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed;

a command generating circuit to generate a first command according to

an operating performance of the first circuit; and

a temperature compensation circuit to measure a t mperature of the first circuit;

wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are adjusted according to the operating performance of the first circuit, and

wherein said temperature compensation circuit issues second, third and fourth command signals according to the first command and a temperature of the first circuit measured by the temperature compensation circuit,

the second circuit sets a frequency of the clock signal in response to the second command signal,

A4 cont.

the third circuit sets a value of the supply voltage in response to the third command signal, and

the fourth circuit sets a value of the substrate bias voltage in response to the fourth command signal.

Sub B2

20. The semiconductor integrated circuit device according to claim 17, wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,

wherein one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined operating speed, and

wherein a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to lower the power consumption of the first circuit.

21. The semiconductor integrated circuit device according to claim 17, wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,

wherein one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is set in order to satisfy a predetermined power consumption, and

wherein a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are set in order to increase the operating speed of the first circuit.

22. A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

A4 cont.

a third circuit to control a supply voltage of the first circuit; and

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed,

wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are adjusted according to the operating performance of the first circuit, and

wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit and the power consumption of the first circuit is controlled according to a remaining quantity of a battery which feeds an electric power to the semiconductor integrated circuit device.

23. The semiconductor integrated circuit device according to claim 18, wherein the first, second and third command signals generated by the command generating circuit are determined according to at least one of an instruction from an operating system, an instruction from an application software, a signal input from outside of the semiconductor integrated circuit device, a signal from a memory or a processing load of the first circuit.

24. The semiconductor integrated circuit device according to claim 18, wherein at l ast one of the command g nerating circuit, the second circuit, the third circuit, and the fourth circuit is formed on another chip rather than a chip where the first circuit is formed.

25. A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a monitor including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of said first circuit is formed; and

wherein values of the frequency of the clock signal, the supply voltage and the substrate bias voltage value are set initially in order to satisfy an operating performance of the first circuit, based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage, and

wherein the clock signal, the supply voltage and the substrate bias voltage are supplied to the monitor, and at least one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is controlled so as to reduce a delay between an output of the monitor and a reference signal.

26. The semiconductor integrated circuit device according to claim 25, further comprising:

a comparator;

wherein the monitor is a delay circuit including inverters connected in series,

wherein the comparator compares an output of the monitor with the reference signal and outputs a first signal when the output of the monitor is later than the reference signal or a second signal when the reference signal is later than the output of the monitor, and

wherein, when the first signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made faster, and, when the second signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made lower.

27. A semiconductor integrated circuit device comprising:

a first circuit having a first MOS transistor of a first conductivity type and a second MOS transistor of a second conductivity type connected in series with the first MOS transistor; and

A4 cont.

a second circuit to control substrate bias voltages supplied to semiconductor regions where the first and second MOS transistors are formed,

wherein said second circuit suppresses variations of an operating frequency of the first circuit by applying the substrate bias voltage, and

wherein a frequency of a clock signal to be supplied to the first circuit and a supply voltage of the first circuit are decided initially for the first circuit whose operating frequency variations are suppressed, based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage.

28. The semiconductor integrated circuit device according to claim 27, wherein the second circuit applies the substrate bias voltage to the semiconductor regions in a range from a forward bias voltage to a reverse bias voltage.

29. The semiconductor integrated circuit device according to claim 27, wherein a first well of the first conductivity type and a second well of the second

conductivity are formed on a substrate of the first conductivity type through an isolation layer of the second conductivity type laid thereb tween, and

wherein the second MOS transistor is formed in the first well and the first MOS transistor is formed in the second well.

30. The semiconductor integrated circuit device according to claim 27, wherein a first well of the first conductivity type and a second well of the second conductivity type are formed on a substrate of the first conductivity type through an insulation layer laid therebetween, and

wherein the second MOS transistor is formed in the first well and the first MOS transistor is formed in the second well.

A4 cont.

31. A semiconductor circuit device comprising:

a first circuit including at least one MOS transistor;

a second circuit means for controlling a frequency of a clock signal to be supplied to the first circuit;

a third circuit means for controlling a supply voltage of the first circuit;

a fourth circuit means for controlling a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed;

means for adjusting the frequency of the clock signal, the supply voltage and the substrate bias voltage according to an operating performance of the first circuit; and

means for deciding initial values of the frequency of the clock signal, the supply voltage and the substrate bias voltage based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage.

32. A semiconductor circuit device according to claim 31, comprising:

command generating circuit means for controlling the second circuit means, the third circuit means and the fourth circuit means; and

wherein the command generating circuit means generates first, second and third command signals according to the operating performance of the first circuit,

the second circuit means sets a frequency of the clock signal in response to the first command signal,

the third circuit means sets a value of the supply voltage in response to the second command signal, and

the fourth circuit means sets a value of the substrate bias voltage in response to the third command signal.

A4 cont.

33. A semiconductor circuit device according to claim 31 comprising:

a first circuit including at least one MOS transistor;

a second circuit means for controlling a frequency of a clock signal to be supplied to the first circuit;

a third circuit means for controlling a supply voltage of the first circuit;

a fourth circuit means for controlling a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed;

means for adjusting the frequency of the clock signal, the supply voltage and the substrate bias voltage according to an operating performance of the first circuit;

means for setting the frequency of the clock signal in accordance with a first command;

means for setting initial values of the supply voltage and the substrate bias voltage based on the set frequency of the clock signal;

means for adjusting the supply voltage and the substrate bias voltage based on the set initial values;

means for evaluating the performance of the first circuit based on the set values of the frequency of the clock signal, the supply voltage and the substrate bias voltage; and

means for adjusting the initial values of the substrate bias voltage based on the evaluated performance of the first circuit.

A4 cont.

34. A semiconductor circuit device according to claim 33, wherein the initial value for the supply voltage is the lowest possible supply voltage for enabling operation based on the set frequency of the clock signal based on a frequency/supply voltage correspondence table.

35. A semiconductor circuit device according to claim 34, wherein the initial substrate bias voltage is set to be an optimum substrate bias voltage to meet a requested performance based on the set frequency of the clock signal and the set supply voltage. --

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated August 28, 2002. Appreciation is expressed for the indication of allowable subject matter in claims 3, 6 and 10.